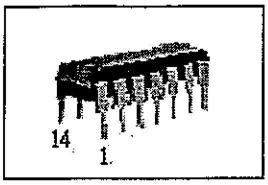
DOS Electronics Pte Ltd

Low Power Low Offset Voltage Quad Comparators F339

Description:

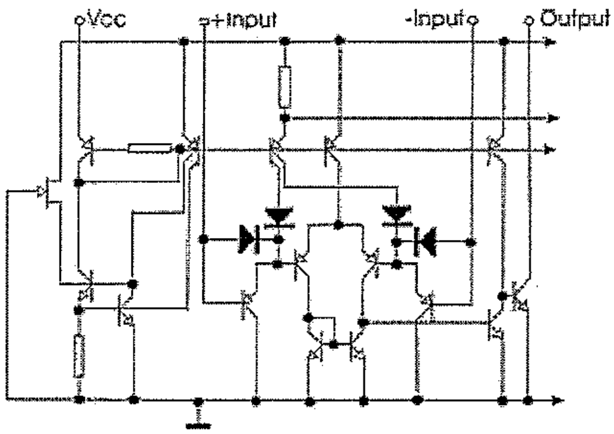
The HT339 consists of four independent precision voltage comparators. These were designed specifically to operate from a signal power supply over a wide range of voltage. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. The HT339 also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.



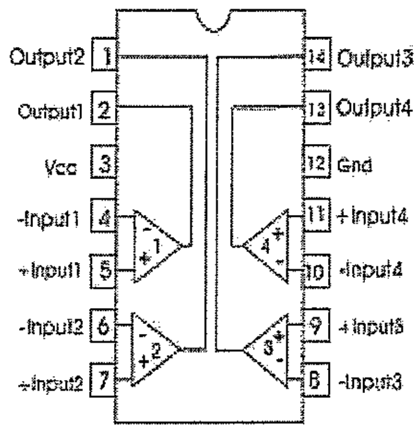
Feature:

- Low input biasing current: 25nA (TYP.).
- Low input offset current: ±5.0nA (TYP.).
- Low output saturation voltage: 130mV.
- Output voltage compatible with TTL,CMOS.

Block Diagram



Pin Configuration



Pin Descriptions

No	Description	Symbol	No	Description	Symbol
1	Output 2	OUT2	8	-Input3	IN3 (-)
2	Output 1	OUT1	9	+Input3	IN3 (+)
3	Supply Voltage	Vcc	10	-Input4	IN4 (-)
4	-Input1	IN1 (-)	11	+Input4	IN4 (+)
5	+Input1	IN1 (+)	12	Ground	GND
6	-Input2	IN2 (-)	13	Output 4	OUT4
7	+Input2	IN2 (+)	14	Output 3	OUT3

Absolute Maximum Ratings

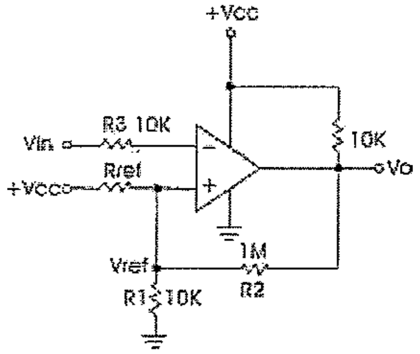
Characteristics	Symbol	Value	Unit
Supply Voltage	Vcc	36 or ±18	V
Differential Input Voltage	V_{IDR}	36	V
Input Voltage	V_{ICMR}	-0.3~Vcc	V
Input Current	I_{SC}	50	
Power Dissipation (*)	P_D	1.0	W
Operating Temperature Range	Tamb	0~75	℃
Storage Temperature Range	Tstg	-65~150	℃

Note (*) : Power dissipation reduces 8 mW/°C for using above Ta=25°C。

Electrical Characteristics (Unless otherwise specified :Vcc=5V, Tamb=25℃)

Characteristics	Test conditions	Symbol	Min	Typ.	Max	Unit
Input Offset Voltage		V_{IO}		±2.0	±5.0	mV
	0℃ ≤ Ta ≤ 70℃				±9.0	
Input Offset Current		I_{IO}		±5.0	±50	nA
	0℃ ≤ Ta ≤ 70℃				±150	
Input Bias Current		I_{IB}		25	250	nA
	0℃ ≤ Ta ≤ 70℃				400	
Input Common-mode Voltage Range		V_{ICR}	0		Vcc-1.5	V
	0℃ ≤ Ta ≤ 70℃		0		Vcc-2.0	
Supply Current	R_L=∞	I_{CC}		0.8	2.0	mA
	R_L=∞, Vcc=30V			1.0	2.5	
Voltage Gain	R_L ≥ 15KΩ, Vcc=15V	G_V	50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V, V_{RL}=5.0V, R_L=5.1KΩ	t_{RES}		300		ns
Response Time	V_{RL}=5.0V, R_L=5.1KΩ	t_{RES}		1.3		ns
Input Differential Voltage		V_{ID}			Vcc	V
Output Sink Current	$V_{IN(-)}$ ≥ 1.0V, $V_{IN(+)}$=0V, V_O ≤ 1.5V	I_{SINK}	6.0	16		mA
Output saturation voltage	$V_{IN(-)}$ ≥ 1.0V, $V_{IN(+)}$=0V, I_{SINK} ≤ 4.0mA	V_{SAT}		130	400	mV
	$V_{IN(-)}$ ≥ 1.0V, $V_{IN(+)}$=0V, I_{SINK} ≤ 4.0mA 0℃ ≤ Ta ≤ 70℃				700	
Output Leakage Current	$V_{IN(-)}$ ≥ 1.0V, $V_{IN(+)}$=0V, V_O = 5.0V	I_{OL}		0.1		nA
	$V_{IN(-)}$ ≥ 1.0V, $V_{IN(+)}$=0V, V_O=30V 0℃ ≤ Ta ≤ 70℃				1000	

Application Circuit

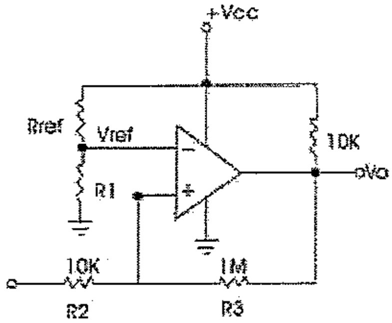


$V_{ref}=\frac{V_{cc}R1}{R_{ref}+R1}$

R3=R1//Rref//R2

$V_H=\frac{R1//R_{ref}}{R1//R_{ref}+R2}[V_o(max)-V_o(min)]$

R2 > Rref//R1

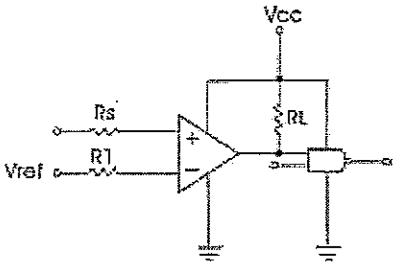


$V_{ref}=\frac{V_{cc}R1}{R_{ref}+R1}$

R2=R1//Rref

Amount of Hysteresis V_H

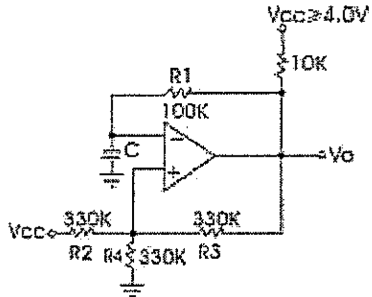
$V_H=\frac{R2}{R2+R3}[V_o(max)-V_o(min)]$

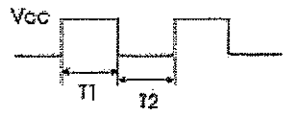


Rs=Source Resistance

R1≈Rs

Logic	Device	Vcc(V)	RL(KΩ)
CMOS	1/4MC14001	+15	100
TTL	1/4MC7400	+5.0	10



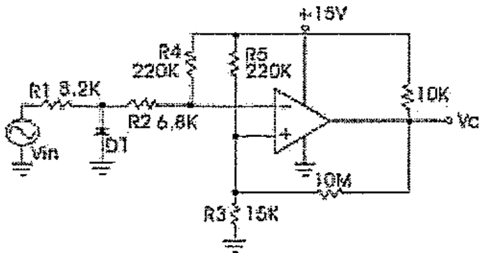


T1=T2=0.69RC

$F=\frac{7.2}{C(uF)}$

R2=R3=R4

R1=R2//R3//R4

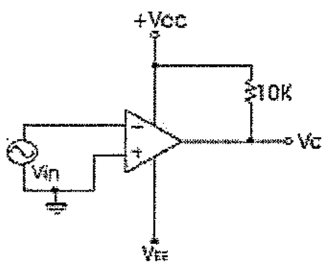


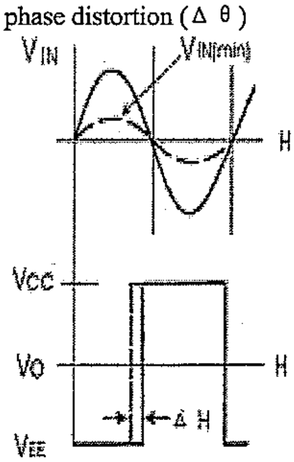
D1 prevents input from going negative by more than 0.6V

R1+R2=R3

R3 ≤ R5/10 for small error in zero crossing

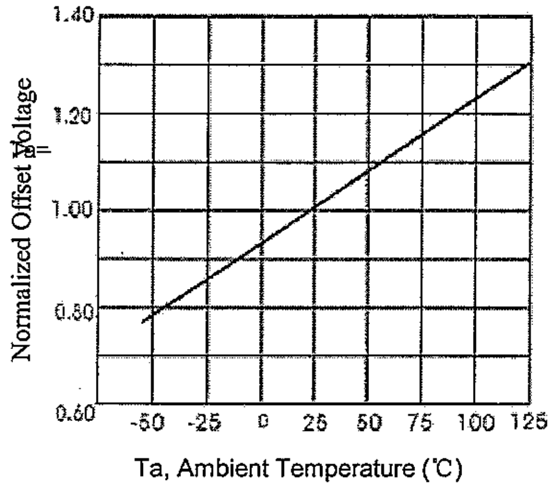
Vin(min)=0.4V peak for 1% phase distortion (Δθ)



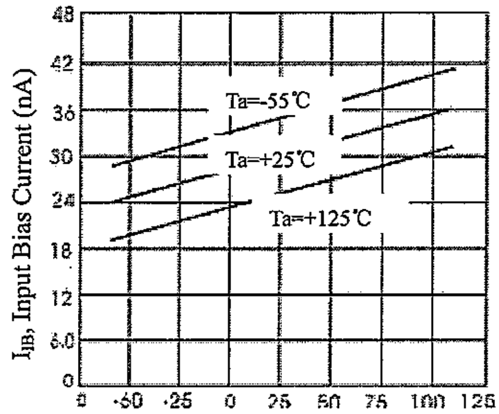


Typical Characteristics Curves:

Input Offset Voltage



Input Bias Current



Output Sink Current and output saturation voltage